WHAT IS CLAIMED IS:

1. An input circuit comprising:

delay means for defining a delay time for at least one logical state of a data signal and thereby delaying the clock signal for the delay time defined; and

a holding circuit for holding the data signal responsive to the delayed clock signal.

2. The input circuit of Claim 1, wherein the delay means defines the delay time such that an edge of the clock signal, on which the data signal is intended to be latched and which is included within a transition interval of the data signal, is delayed to a point in time after the transition interval of the data signal is over.

3. The input circuit of Claim 2, wherein the delay means comprises:

a comparator for comparing the edge of the clock signal, on which the data signal is intended to be latched, to at least one of leading and trailing edges of the data signal; and

a delay circuit for defining the delay time based on a result of comparison performed by the comparator.

4. The input circuit of Claim 2, wherein the delay means comprises:

a comparator for comparing the edge of the clock signal, on which the data signal is intended to be latched, to lead-

ing and trailing edges of the data signal;

a first delay circuit for defining the delay time for a logically high state of the data signal based on a result of comparison, performed by the comparator, between one of the leading edges of the data signal and the edge of the clock signal;

a second delay circuit for defining the delay time for a logically low state of the data signal based on a result of comparison, performed by the comparator, between one of the trailing edges of the data signal and the edge of the clock signal; and

a selector for selecting the delay time defined by the first delay circuit when the data signal is in the logically high state or the delay time defined by the second delay circuit when the data signal is in the logically low state.

5. The input circuit of Claim 3 or 4, wherein the delay circuit defines the delay time based on the result of comparison performed by the comparator and a setup time for correctly latching the data signal.

6. An output circuit comprising:

a driver including a plurality of devices outputting a data signal, the total drivability of the devices being controllable; and

a controller, responsive to a signal representing a transition interval length of the data signal, for increasing

or decreasing the drivability of the driver.

7. The output circuit of Claim 6, wherein the controller receives the signal, representing the transition interval length of the data signal, from an input circuit to which the data signal is output from the output circuit.

Add B2

Add C3